MODELING THE EFFECT OF VELOCITY SATURATION IN NANOSCALE MOSFET

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To my wonderful parents and family, for their guidance, support, love and enthusiasm. I am so thankful for that blessing and for the example you both are to me over the years. I would not have made it this far without your motivation and dedication to my success. Thank you, mom and dad, I love you both.

ACKNOWLEDGEMENTS

First of all, I am thankful to my supervisor, Associate Professor Dr Razali Ismail for his precious insight, guidance, advice and time. I would like to take this opportunity to record my sincere gratitude for his supports and dedication throughout the years.

My thankfulness also goes to my manager in Intel Penang Design Center, Mr Ravisangar Muniandy. His immense support and encouragement was keeping me going during the times when I was encountering problems at every turn. I wish to express my most heartfelt thankre abroad and even made themselves available when I had questions after our meeting.

I thank the many good friends I met here, Kaw Kiam Leong, Ng Choon Peng, Lee Zhi Feng and many others for the encouragement and unforgettable memories. They have always given me the chance to discuss my academic issues as well as my personal issues. Without them, I could not have been completed my study. Very valuable advice was also given by fellow friend, Dr Kelvin Kwa for his sharing of experience, sachets of tea and coffee, books and advices. Also, thank to my friends Sim Tze Yee, Liu Chin Foon, Liew Eng Yew, Gan Hock Lai and Alvin Goh Shing Cyhe. I cherish the ideas they have given me, their support and warmhearted friendship.

On a personal note, I would like to thank my family who has always supported me and the encouragement they have given me.

ABSTRACT

MOSFET scaling throughout the years has enabled us to pack million of MOS transistors on a single chip to keep in pace with Moore's Law. The introduction of 65 nm and 90 nm process technology offer low power, high-density and high-speed generation of processor with latest technological advancement. When gate length is scaled into nanoscale regime, second order effects are becoming a dominant issue to be dealt with in transistor design. In short channel devices, velocity saturation has redefined the current-voltage (*I-V*) curve. New models have been modified and studied to provide a better representation of device performance by understanding the effect of quantum mechanical effect. This thesis studies the effect of velocity saturation on transistor's internal characteristic and external factor. Velocity saturation dependence on temperature, substrate doping concentration and longitudinal electric field for n-MOSFET are investigated. An existing current-voltage (*I-V*) compact model is utilized and modified by appending a simplified threshold voltage derivation and a more precise carrier mobility model. The compact model also includes a semi empirical source drain series resistance modeling. The model can simulate the performance of the device under the influence of velocity saturation. The results obtained can be used as a guideline for future nanoscale MOS development.

ABSTRAK

Penskalaan mendadak MOSFET dari tahun ke tahun selari dengan Hukum Moore membolehkan berjuta-juta transistor dimuatkan ke dalam serpihan silikon. Berikutan pengenalan teknologi proses 65 nm and 90 nm, arus pembaharuan yang dramatik telah membawa kepada penumpuan pemproses yang pantas, berkuasa rendah dan berdensiti tinggi dengan pendekatan teknologi terbaru. Kesan tertib kedua menjadi satu isu dominan untuk ditangani dalam rekaan transistor apabila panjang saluran mencecah nanometer. Salah satu daripandanya ialah halaju tepu yang telah membawa definasi baru bagi ciri-ciri voltan and arus *(I-V)* dalam peranti saluran/kanal pendek. Model-model baru telah diperkenalkan untuk memberi representasi prestasi yang jelas dengan mengambil kira teori fizik kuantum. Penyelidikan ini bertujuan untuk meneliti kesan halaju tepu ke atas faktor luaran dan dalam ke atas transistor. Hubungan hanyut dan halaju tepu dengan suhu, kepekatan pendopan and medan elektrik diperhatikan. Model voltan-arus *(I-V)* sedia ada digabungkan bersama model kebolehgerakan elektron yang lebih terperinci untuk menganalisis parameter-parameter di atas. Model padat tersebut juga mengandungi model perintang bersiri sumber-salir semiempirik. Persamaan voltan ambang telah diterbitkan dan berupaya memberikan ketepatan yang sama dengan silikon sebenar dan dibuktikan dengan teknik kesesuaian pemadanan. Melalui pendekatan simulasi, model-model ini dapat memberi prestasi peranti di bawah pengaruh halaju tepu. Keputusan penyelidikan ini boleh digunakan sebagai panduan untuk perkembangan MOS pada masa depan.

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LIST OF ABBREVIATIONS

ASIC	-	Application Specific Integrated Circuits
BSIM3v3	-	Berkeley Short-Channel IGFET Model Three Version Three
CMOS	-	Complementary Metal Oxide Semiconductor
CSV	-	Comma Separated Values
EDA	-	Electronic Design Automation
FET	-	Field Effect Transistor
GCA	-	Gradual Channel Approximation
GUI	-	Graphical User Interface
IC	-	Integrated Circuit
MOS	-	Metal Oxide Semiconductor
MOSFET	-	Metal Oxide Semiconductor Field Effect Transistor
NMOS	-	n-channel MOSFET
PMOS	-	p-channel MOSFET
SOE	-	Second Order Effects
VLSI	-	Very Large Scale Device
VSR	-	Velocity Saturation Region
GHz	-	Giga Hertz
GaAr	-	Galium Arsenide
InP	-	Indium Phosphide

k	-	Boltzmann’s constant
L	-	Channel length
S	-	Spacer thickness
Si	-	Silicon
S/D	-	Source and Drain

LIST OF SYMBOLS

A	-	Ampere (unit for current)
Cu_2S	-	Copper Sulfide
C_{ox}	-	Gate oxide capacitance
E	-	Electric Field
E_{eff}	-	Effective transverse electric field
E_c	-	Critical electric field
E_g	-	Energy bandgap variation
ε_{Si}	-	Dielectric permittivity of the silicon
ε_{ox}	-	Dielectric constant of the oxide
I-V	-	Drain current versus drain voltage
I_{ds}	-	MOSFET drain current
I_{dsat}	-	Drain current saturation
InP	-	Indium Phosphide
J_n	-	Drift current density
k	-	Boltzmann's constant
L	-	Channel length
μ_{eff}	-	Effective mobility
μm	-	micrometer
μ_c	-	Coulombic scattering
μ_{ph}	-	Phonon scattering

μ_{sr}	-	Surface roughness scattering
ϕ_f	-	Fermi potential
ϕ_{fp}	-	Fermi surface potential for p-type semiconductor
ϕ_{fn}	-	Fermi surface potential for n-type semiconductor
N_A	-	Acceptor doping concentration
N_D	-	Receptor doping concentration
N_I	-	Number of electrons per unit area in the inversion layer
N_c	-	Density of states function in conduction band
N_v	-	Density of states function in valence band
n_i	-	Intrinsic carrier concentration
nm	-	nanometer
n	-	Free electron density
p	-	Fuchs factoring scattering
ρ	-	Effective resistivity
Q_{tot}	-	Effective net charges per unit area
Q_I	-	Inversion charge per unit area
Q_n	-	Inversion Charge
R_{sd}	-	Source and drain resistance
R_d	-	Source resistance
R_{ext}	-	Extrinsic resistance
R_{int}	-	Intrinsic resistance
R_{ac}	-	Accumulation resistance
R_{sp}	-	Sreading resistance
R_{sh}	-	Sheet resistance
R_{co}	-	Contact resistance

S	-	Spacer thickness
ϕ_{ms}	-	Work Function
t_{ox}	-	Oxide thickness
v_d	-	Drift velocity
V	-	Voltage (unit for potential difference)
V_{ds}	-	Drain voltage
$V_{dsat.}$	-	Drain voltage saturation
V_c	-	Critical Voltage
V_{FB}	-	Flat band voltage
V_{gs}	-	Gate Voltage
V_t	-	Threshold Voltage
ν_{sat}	-	Carrier saturation velocity
W	-	Channel width
x_{dT}	-	Depletion width
x_j	-	Junction depth
χ	-	Oxide electron affinity
Z	-	Averaged inversion layer width
Z_{cl}	-	Classical channel width
Z_{QM}	-	Quantum mechanically broadened width
Ω	-	ohm (unit for resistivity)

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CHAPTER I

INTRODUCTION

1.1 Background

Silicon is one of the semiconductor materials which is commonly used in chip manufacturing to make integrated circuit from miniaturized transistor. Metal Oxide Semiconductor (MOS) transistor have shrunk from a micrometer into sub 100 nm regime with transistor scaling, which increases the number of transistor per size by a factor of two every 18 months in accordance to Moore's Law (Moore, 1965). Many improved lithographic and semiconductor fabrication equipments were designed to be on track with the curve and one step ahead of the technology. So far, Moore's law has been a valuable way of describing the general progress of integrated circuits and the number of transistors fitted into each generation of Intel processors, as shown in Figure 1.1.

In silicon chip manufacturing, feature size and wafer size is the two most important parameter as they determined the cost of a plant and production line equipments. Presently, 300 mm wafers is the largest silicon wafers which produce more than double as many chips as the older 200 mm wafers. Since the end of 2005, Intel is the first manufacturer offering single and core 2 duo processors based on 65 nm production technologies. 65 nm generation transistors come with gates that are able to turn a transistor on and off measuring only 35 nm which is roughly 30 percent smaller than 90 nm technology gate lengths. Intel claims that 65 nm transistors cut current leakage by four times compared to previous process technology. According to Figure 1.2, new technology generation is introduced every 24 months and this

successfully extends their 15-year record of mass production in Intel. As performance technology improves, the gate length start to get smaller than predicted by the ideal feature size trend of each process technology. This allows higher transistor density, squeezing more of them on a single chip. The roadmap of semiconductor from 1977 to 2018 can be seen in Appendix B and Appendix C.

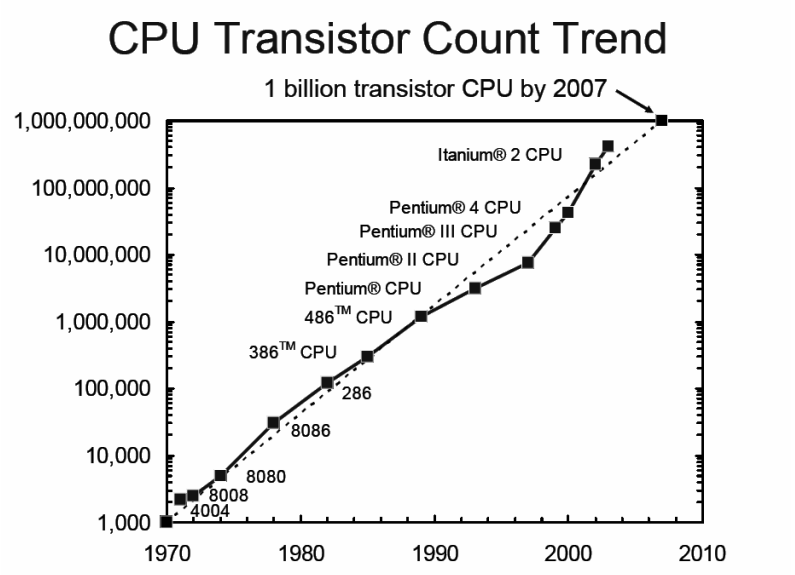

Figure 1.1 Growth of transistor counts for Intel processors accordance to Moore's Law

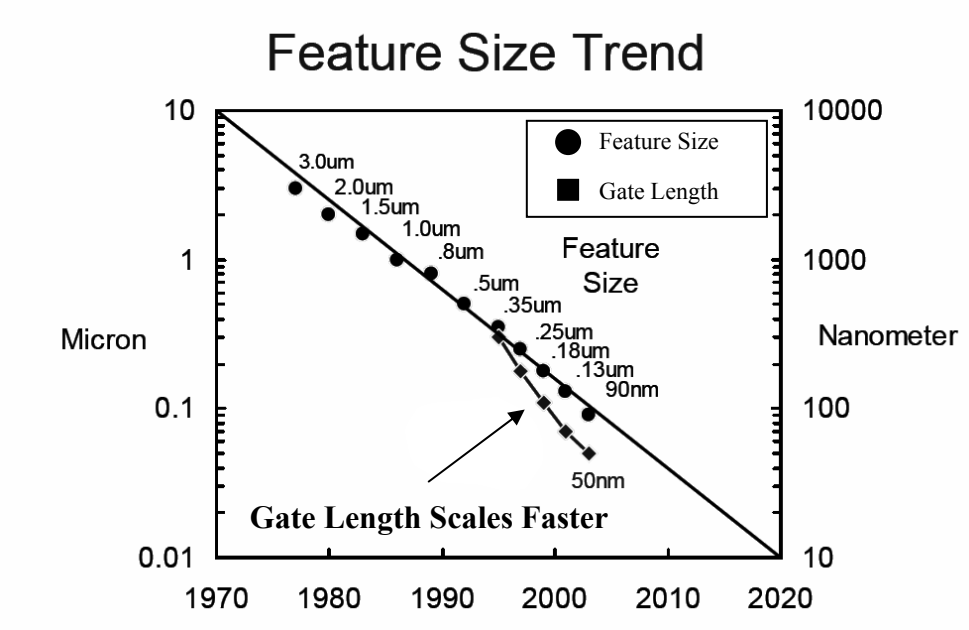

Figure 1.2 Feature Size Growth

In nanoscale dimension, new problems began to occur. The magnitude of the electric field is comparably higher in short channel devices than long channel devices where the channel length is comparable to the depletion region width of the drain and source. Here, Secondary Order Effect (SOE) exists and must be considered to model the generation of a more precise short channel Metal Oxide Semiconductor Field Effect Transistor (MOSFET). Velocity saturation is a vital parameter of the SOE which occur in high electric field.

At low electric field, the drift velocity of electron, v_d is proportional to the electric field, E as shown in Eq. (1.1).

$$v_d = \mu_{eff} E \tag{1.1}$$

where μ_{eff} is the effective mobility. When the electric field applied is increase, nonlinearities appear in the mobility and carriers in the channel will have an increased velocity. In high field, charge carriers gain and lose their energy rapidly particularly through phonon emission until the drift velocity reaches a maximum value called velocity saturation. Velocity saturation in MOSFET will yield a smaller lower drain current and voltage. A cross section of a MOSFET is illustrated in Figure 1.3. This research focuses on the role of velocity saturation has on the characteristic of MOSFET in term of the carrier velocity field, carrier doping concentration, drain current versus drain voltage curve. Intel proprietary software is used to generate the experimental drain current versus drain voltage characteristic for 90nm generation of MOSFET. After parameter extraction is carried out, several compact models are employed to study the effect of velocity saturation and the impact of high electric field. The modified device models will be able the predict behavior of electrical devices based on fundamental physics. Characteristics and gives us the mobility and the drift velocity of the electrons versus transverse and longitudinal electric field respectively.

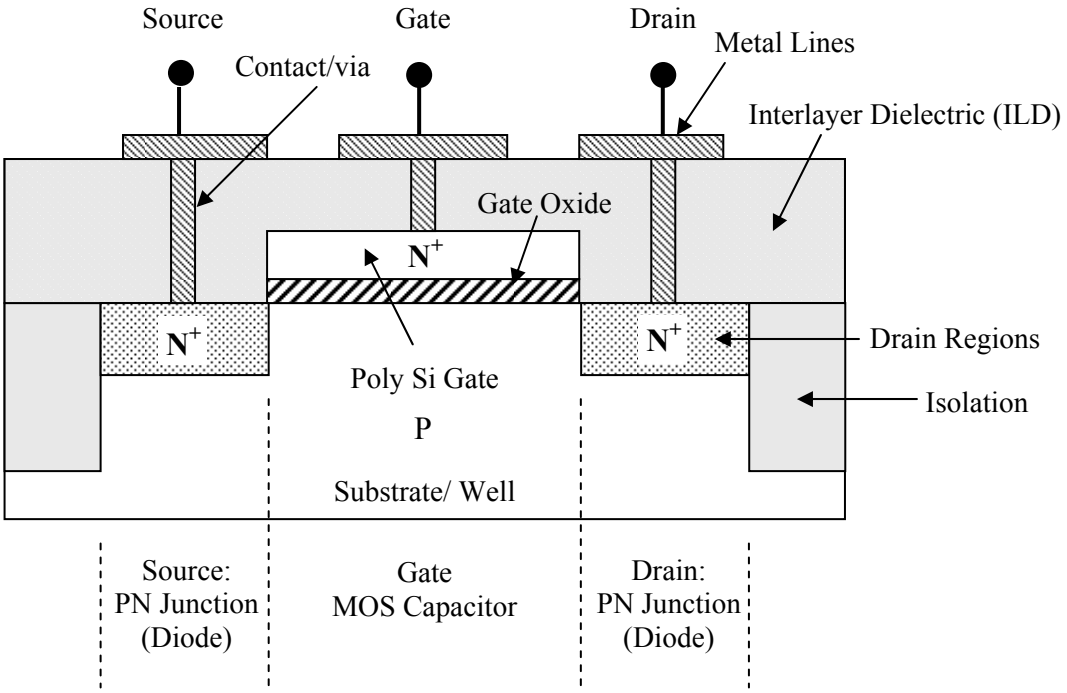

Figure 1.3 MOSFET Source to Drain Cross Section

1.2 Problem Statements

This research utilizes a newly developed short channel models to study velocity saturation in 90 nm process technology and reports the results it has on the transistor basic characteristic. Questions that are bound to be answered through the high field analysis are:

(i) What is velocity saturation?

(ii) What is the different between short and long channel devices? What is the limitation of nanometer MOSFET?

(iii) How does velocity saturation affect the transistor?

(iv) What models can be represented to predict the characteristics and behaviors of Complementary Metal Oxide Semiconductor (CMOS) transistor in nanometer dimension?

(v) What are the limitations of conventional long channel models?

1.3 Objectives

The following are the objectives of this study.

(i) To understand high field effects in nanoscale transistor in 90nm process technology.
(ii) To formulate simple analytical and semi-empirical equations for device model applicable to nanoscale devices by taking into account velocity saturation.
(iii) To analyze velocity saturation effects on temperature, doping concentration, longitudinal and transverse electric field.

1.4 Research Scope

The goal of this research is to investigate the role and characteristic of velocity saturation on the following parameters.

(i) Longitudinal electric field
(ii) Transverse electric field
(iii) Doping concentration
(iv) Mobility
(v) Drain current and voltage (*I-V)* curve
(vi) Temperature

The research is divided into three major phases. In the beginning, literature review and previous researches in this field is carried out. Strengths and weaknesses of available model and equations are compared. The second phase begins with the modeling based on the literature review. A semi-empirical model for velocity saturation due to high field mobility degradation is presented. Best fit model parameters are extracted from the experimental results. The results compared with a

set of published experimental data points and validated. The final phase is preceded with analysis incorporating all the derived and modified models.

Future improvements and suggestion for the model are presented at the end of the thesis. N-channel MOSFET with polysilicon gate is used in this research. The I_{ds} compact model is derived by studying and analyzing Berkeley Short-Channel IGFET Model 3 Version 3 (BSIM3v3) standard (Berkeley, 2005). The one region equation from linear to saturation is based on the modification of the conventional long channel model with the addition of second order effects, each parameter with its physical meanings. Other semi empirical models include threshold voltage, mobility and source drain series resistance.

1.5 Contributions

The semiconductor industry particularly microchip industry strives to develop high performance processor which is capable to cater for the demanding market. MOSFET-based integrated circuits have become the dominant driving force in the industry. It is important for the research and development's designer team to investigate how transistor behaves differently in nanometer dimension. These characteristic includes the electric field, carrier velocity field, carrier mobility, carrier concentration, carrier in saturation velocity region and drain current versus drain voltage in short channel devices.

The modified short channel models are able to overcome the limitations of previously long channel analytical and semi empirical models without velocity saturation. It is also the interest of this study to find out the critical voltage and electric field when velocity saturation appears. Based on this evaluation, it can provide a guideline for designers in term of graphical representation on figures and as well as parameter dependency relationship on the mobility behaviour, including threshold voltage, doping concentration and temperature. Designer can examine the behavior of the device when it is saturated at high electric field under specific

temperature and doping concentration. They can improve their design after a thorough testing to prevent device breakdown.

Long channel *I-V* (current voltage) model is based on one dimensional theory. The modified short channel model is more accurate for nanoscale MOSFET than long channel model which cover Poisson's equation using gradual channel approximation and coherent Quasi 2 Dimensional (2D) analysis in the velocity saturation region. We have included the drain source resistance as well as the high longitudinal electric field effects into the *I-V* model. Furthermore, the threshold voltage model also includes the aspect of non ideal effects such as short channel threshold voltage shift and narrow width effects. In addition, through these calculated results, a bigger picture is given on how velocity saturation can be sustained. On top of that, several enhancement and insight is discussed to overcome the challenges in MOSFET design particularly the reduced drive strength. By investigating the effects of velocity saturation, the author attempts to give general guidelines of how parameters should be chosen.

1.6 Thesis Organization

This thesis consists of 8 chapters. Chapter 1 introduces the background of this research. The problem statements, research objectives, research scope, research contributions and thesis organization are also provided. Chapter 2 provides an overview of the literatures reviewed throughout the research. A detailed description on velocity saturation effects is presented. Previous long channel model characteristics and related research are summarized.

Chapter 3 deals with the work flow of this research. It also introduce the modeling process as well as the Intel Proprietary Schematic Editor and Circuit Simulator. Chapter 4 marks the beginning of the proposed models formulation with the introduction of threshold voltage modeling. Chapter 5 discusses about the electron mobility model in MOS inversion layer. A comprehensive semi empirical

drain current and voltage model is explained in Chapter 6 by studying the long channel characteristics and short channel effects. In addition, this chapter also includes the derivation of source and drain resistance equation which normally omitted in long channel devices. In Chapter 7, we study the velocity field model which describes the effects of high vertical and lateral field in inversion layer pinch off and velocity saturation.

In Chapter 8, the calculated data is observed and validated against the experimental data generated from simulations to investigate effects of velocity saturation. Analysis was carried out on the simulated results and the findings are discussed. Finally, Chapter 9 concludes the thesis with summary of contributions and suggestions for possible future development.

Several newly developed models are modified and employed to analyze the characteristics and behaviors of transistor in sub-100 nm. They are the threshold voltage model, physically based model for effective mobility and compact *I-V*, velocity field model and source drain resistance model. It is vital to investigate the physical insight into the device's operating principles at high field to diminish hot carrier effect and avoid catastrophic breakdown of the device via punchthrough. The abovementioned models are improvement upon existing long channel models and include various effects discussed in previous chapters.

Intel Proprietary Schematic Editor and Circuit Simulator are used to generate experimental data. The relevant parameters are then extracted from the *I-V* curve. Finally, the modified models are utilized to characterize the effects of velocity saturation and effective mobility on drain voltage, gate voltage, temperature and doping concentration. Simulated results show that the temperature effect on velocity saturation depends on the predominant scattering mode. It is shown that at high fields where surface roughness is predominant, the mobility has a negative temperature coefficient and the velocity saturates at lower temperatures. Substrate doping concentration changes the transverse field and scattering modes for a given gate bias, and hence the saturation velocity is achieved at different longitudinal fields

9.2 Recommendations for Future Work

(i) The V_T model can be modified to account for nonuniform channel doping profile. When the MOSFET channel is nonuniformly doped, designer has the flexibility to tailor the desired threshold voltage and the off current requirement. Among the advanced MOSFET variation is threshold voltage adjustment implantation, punchthrough implantation and halo implantation.

(ii) The electron mobility model can be extended into strained and doped silicon transport. The presence of a Ge alloy in strained silicon has additional implications for the effective mobility over the universal

mobility curve. Alloy scattering can be added describe the carrier collision with the SiGe alloy substrate.

(iii) The implication of velocity saturation effects on PMOS can also be examined. With the simulated results, research can be carried out in order to observe the hot carrier effects focusing on CMOS in processor particularly at high temperature operation.

(iv) By using PSpice Model Editor, the derived model can be exported to the library and configured to simulate the design output for DC analysis. Instead of using Microsoft Excel, the analytical and semi empirical models can be redefined into SPICE models and added into a circuit as a schematic symbol to perform basic simulation.

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